United States Patent [19]

Takemoto et al.

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[54] **OXIDE WALLED EMITTER**

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Related U.S. Application Data

[63] Continuation of Ser. No. 231,460, Feb. 4, 1981, abandoned.

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[52] **U.S. Cl.** **357/50**; 357/34; 357/55; 357/59; 357/20

[58] **Field of Search** 357/50, 55, 89, 34, 357/20

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,160,991	7/1979	Anantha et al.	357/50
4,214,315	7/1980	Anantha et al.	357/50
4,231,819	11/1980	Raffel et al.	357/50
4,255,207	3/1981	Nicolay et al.	357/55
4,269,636	5/1981	Rivoli et al.	357/55
4,318,751	3/1982	Horng	357/50

OTHER PUBLICATIONS

Cosand, "Very High Speed . . . Bipolar . . . ", IEEE International Electron Dev. Meeting, Technical Digest, Dec. 1973, pp. 35–37.

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[57] **ABSTRACT**

A semiconductor integrated circuit device in which the side surfaces of an emitter of an oxide isolated bipolar transistor are surrounded with insulating compounds or regions so that the capacitance between the emitter and base is lowered and a base is formed by the self-alignment so that the influence of an active base between an external base and the emitter can be made negligible. Thus the base resistance and parasitic capacitance are lowered.

7 Claims, 21 Drawing Figures